**Microprocessor and Computer Architecture Laboratory**

**UE19CS256**

**4th Semester, Academic Year 2020-21**

Date:3-4-2020

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Week#\_\_\_\_9\_\_\_\_\_\_\_Program Number: \_\_1\_\_\_\_

Title of the Program

1. Consider a direct mapped cache of size 16 KB with block size 256 bytes. The size of main memory is 128 KB. Find Number of bits in tag. Randomly generate 10 addresses and find hit rate and miss rate.

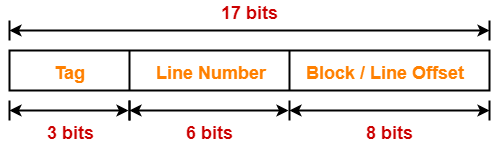
**Solution:**

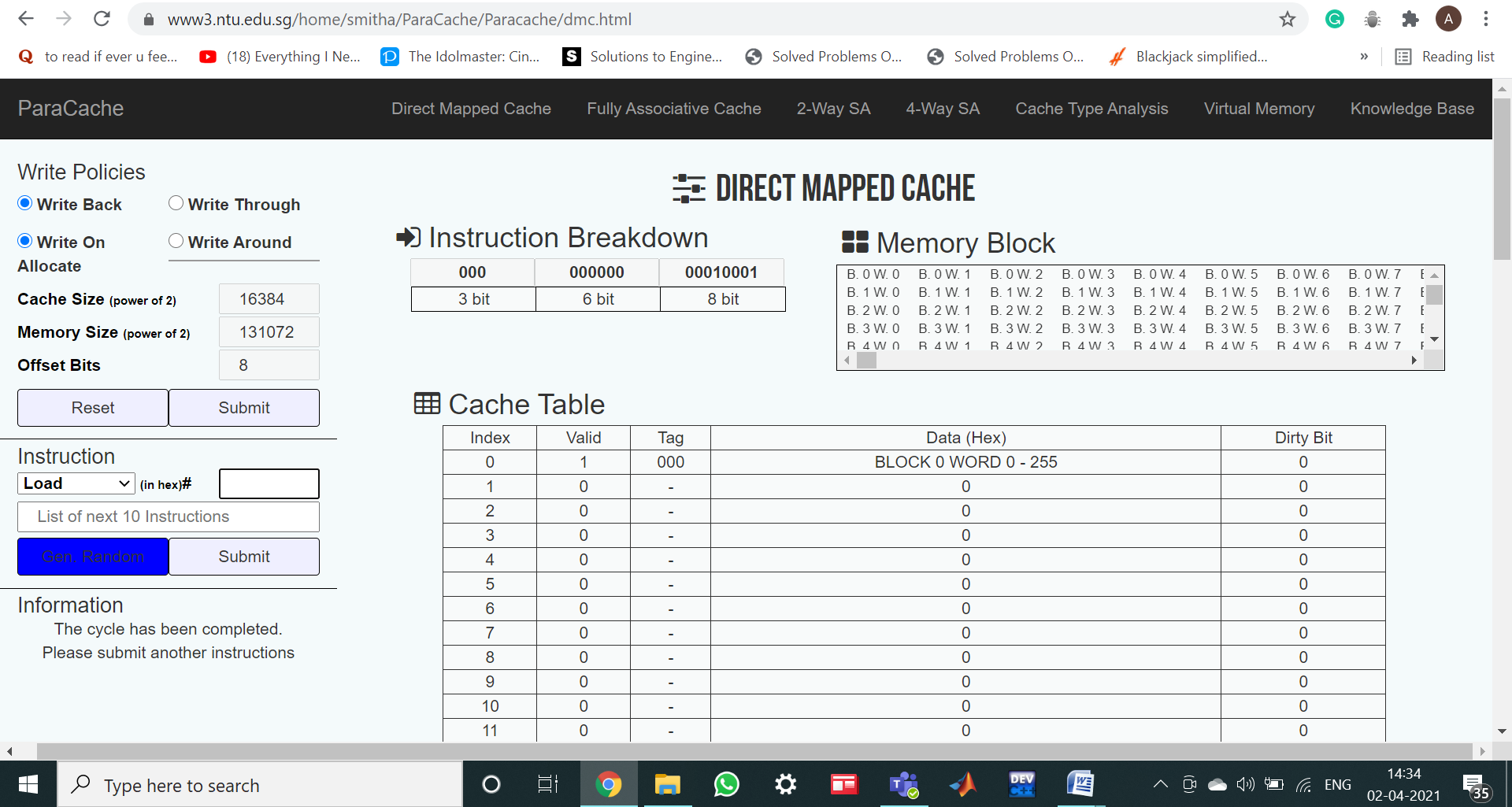
**Given-**

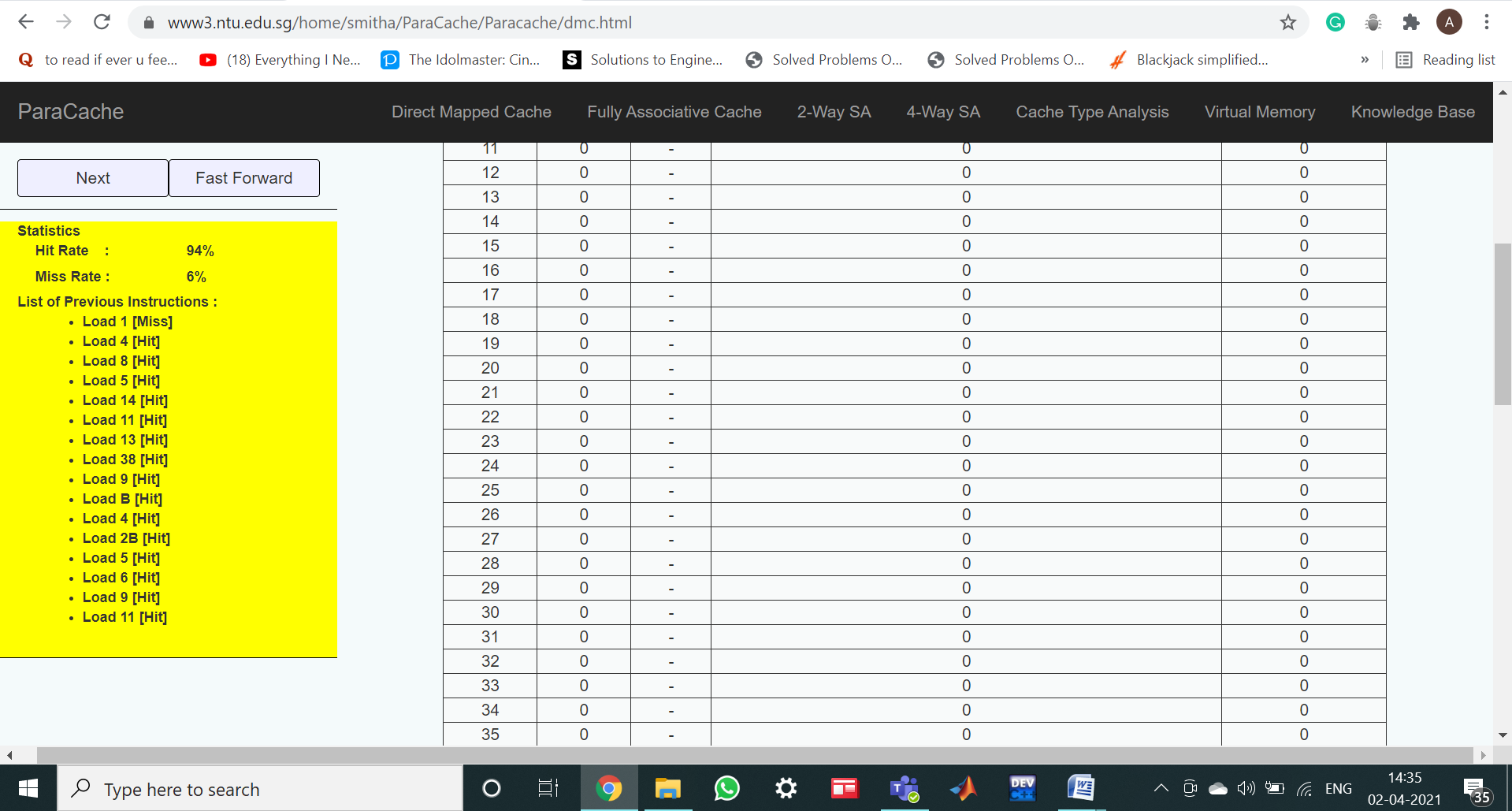
**Cache memory size = 16 KB**

**Block size = Frame size = Line size = 256 bytes**

**Main memory size = 128 KB = 2^17**

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| Name: | SRN: | Section: |

Week#\_\_\_\_9\_\_\_\_\_\_\_Program Number: \_\_2\_\_\_\_

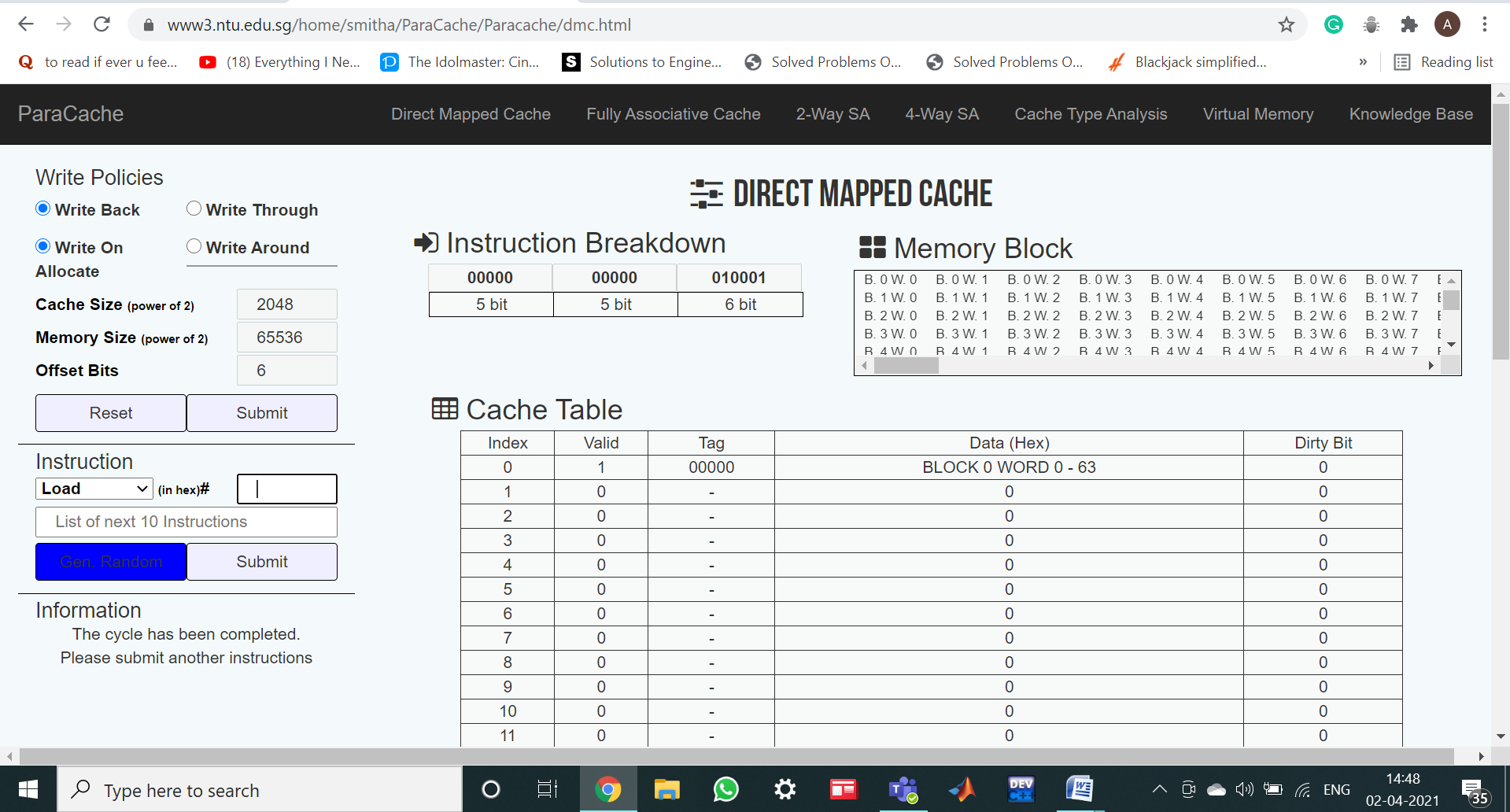
2.computer system uses 16-bit memory addresses. It has a 2K-byte cache organized in a direct-mapped manner with 64 bytes per cache block. Assume that the size of each memory word is 1 byte.

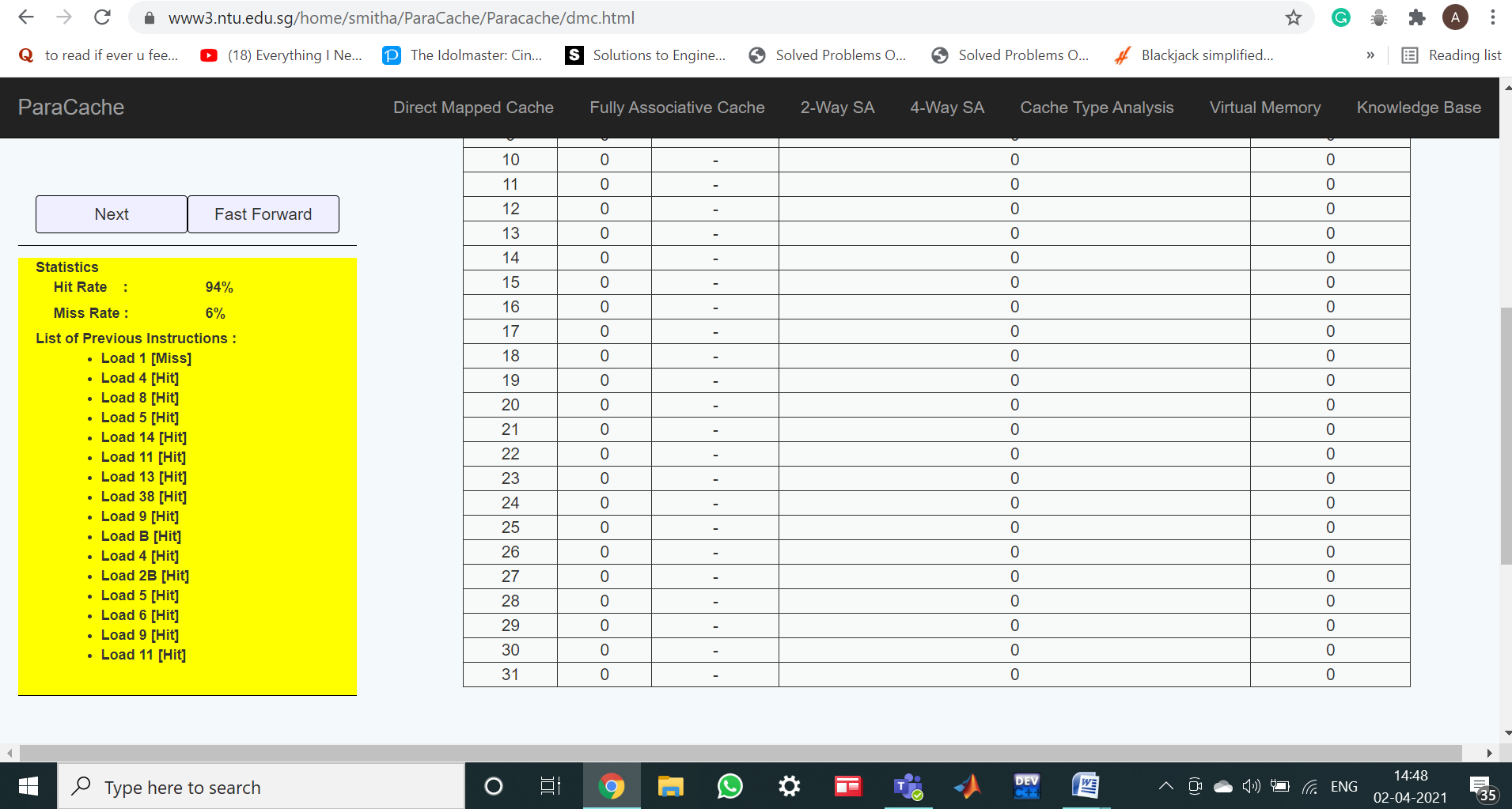
a) Calculate the number of bits in each of the Tag, Block, and Word fields of the memory address.

(b) When a program is executed, the processor reads data sequentially from the following word addresses: **128, 144, 2176, 2180, 128, 2176**

All the above addresses are shown in decimal values. Assume that the cache is initially empty. For each of the above addresses, indicate whether the cache access will result in a hit or a miss.

1. Tag **= 5, *Block* = 5, *Word* = 6**





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| Name: | SRN: | Section: |

Week#\_\_\_\_9\_\_\_\_\_\_\_Program Number: \_\_3\_\_\_\_

3.Consider a 2-way set associative cache of size 16 KB with block size 256 bytes. The size of main memory is 128 KB. Find Number of bits in tag.

Randomly generate 10 addresses and find hit rate and miss rate.

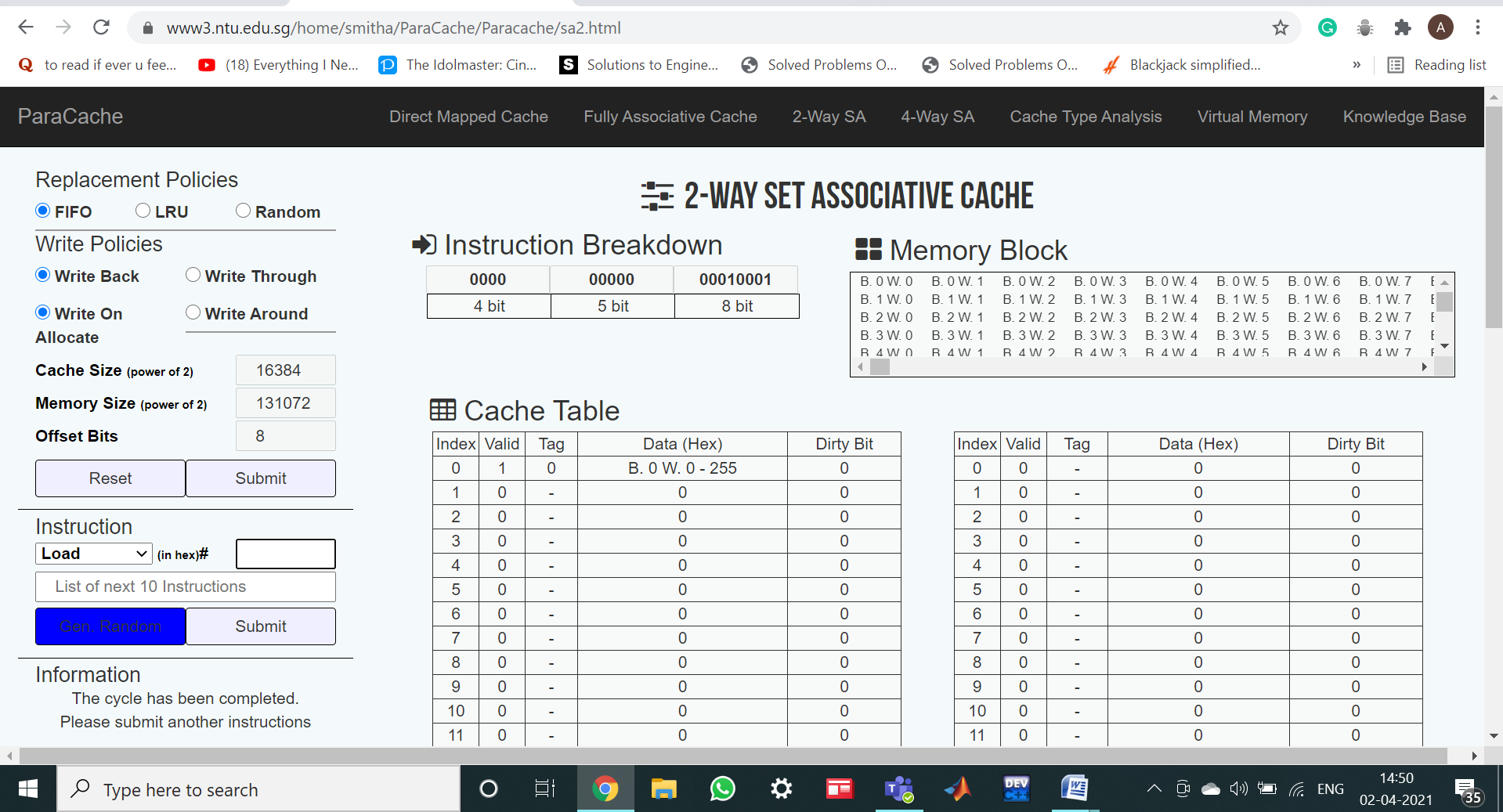
**Solution:**

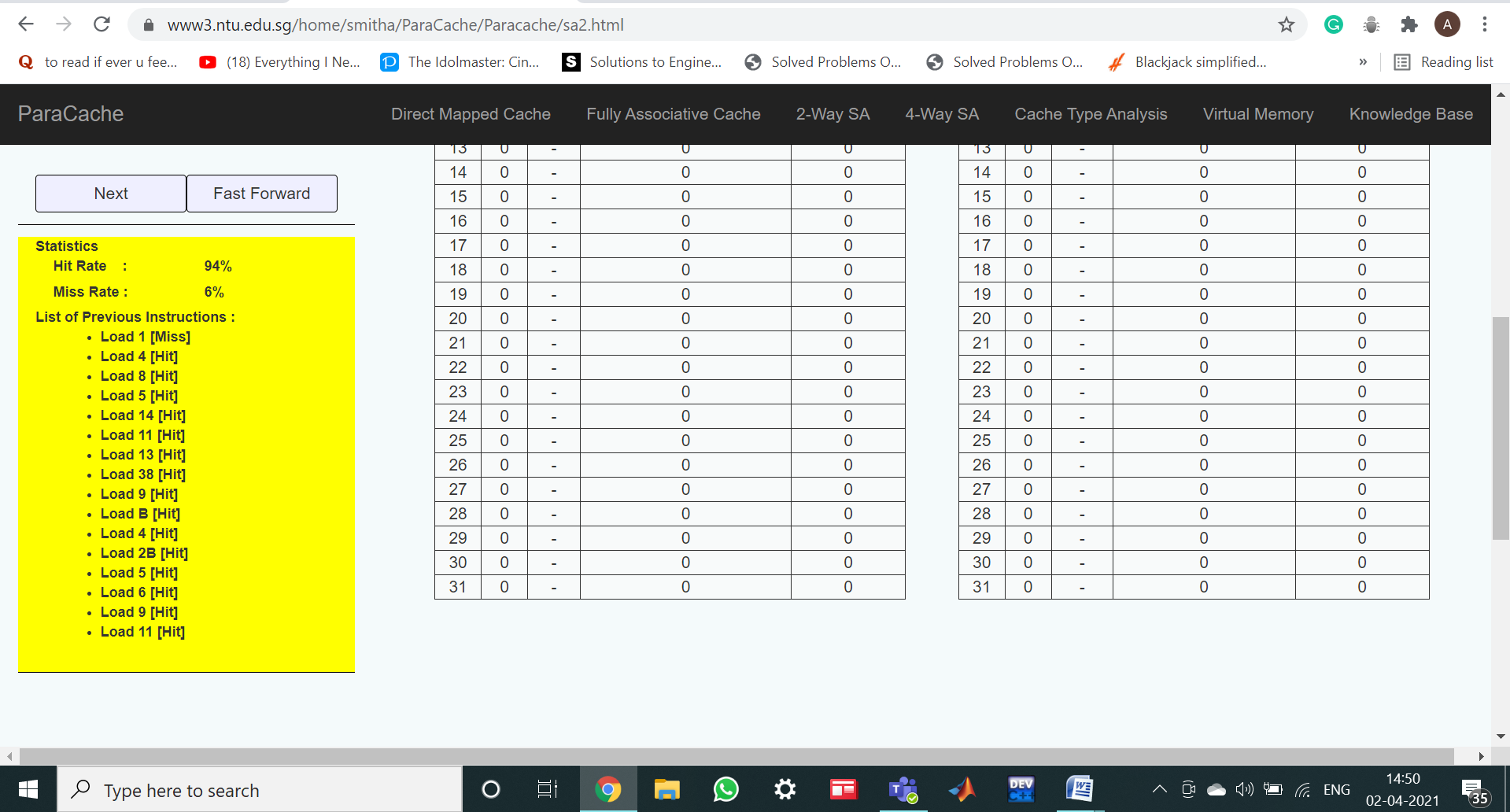
Given- •Cache memory size = 16 KB

•Block size = Frame size = Line size = 256 bytes

•Main memory size = 128 KB = 217 bytes

Thus, Number of bits in physical address = 17 bits

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| Name: | SRN: | Section: |

Week#\_\_\_\_9\_\_\_\_\_\_\_Program Number: \_\_4\_\_\_\_

4.Consider a main memory having 64 byte capacity and cache memory of 8 bytes initially empty

The following addresses are generated by the CPU.All values in hexadecimal

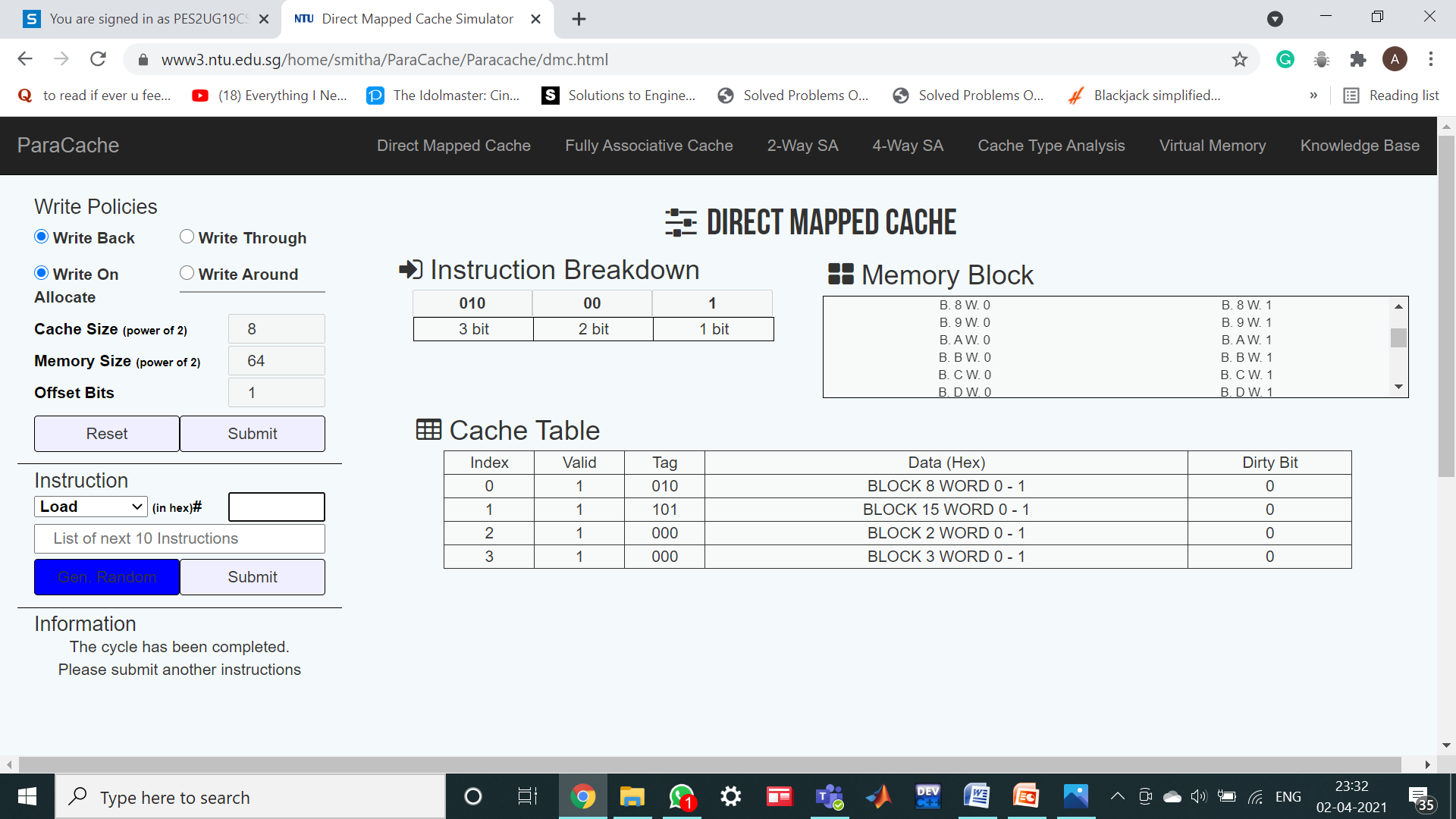
Clearly label data that is replaced in cache lines

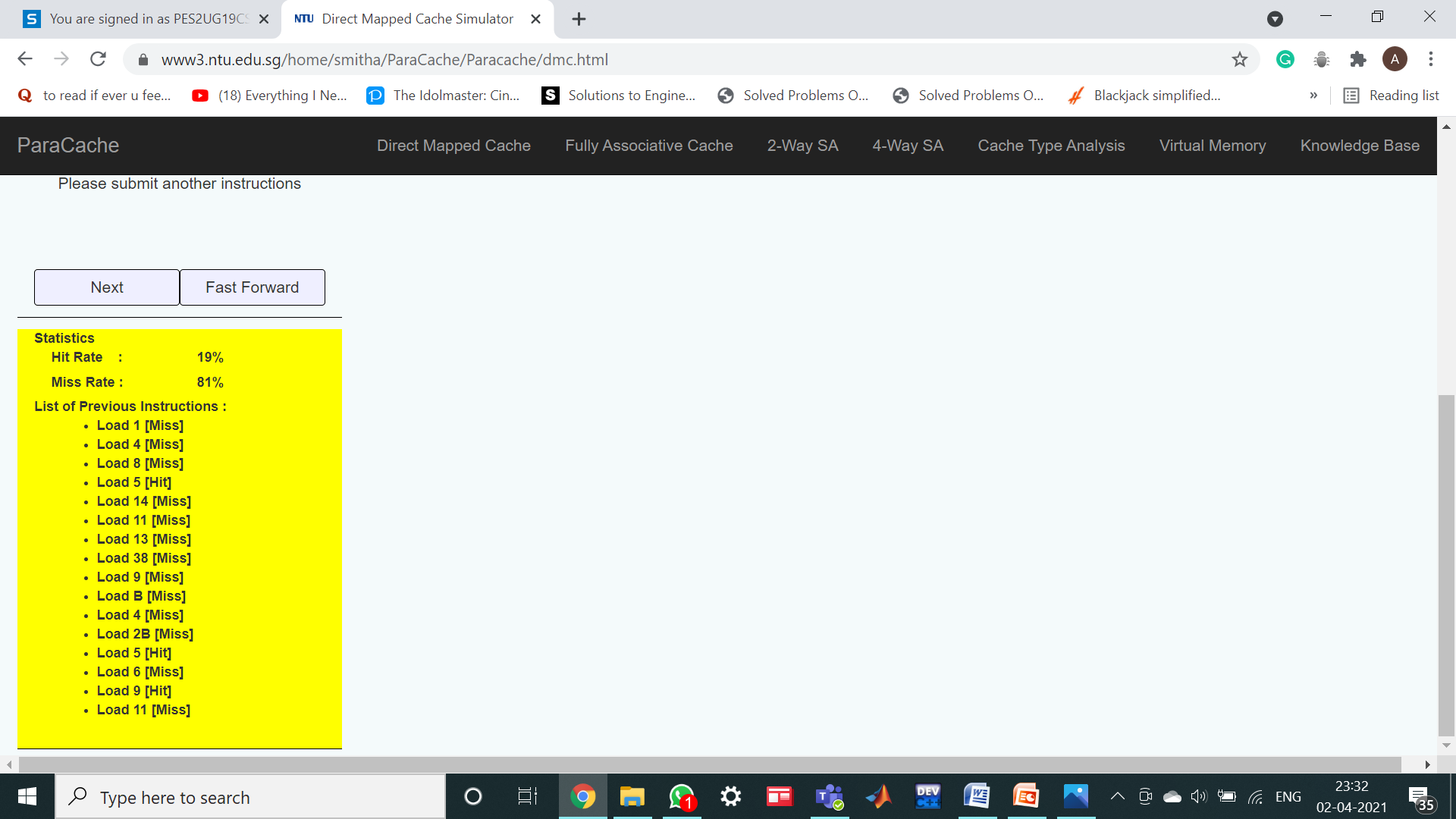
Show the cache memory table and filled data in the cache lines of block size 1 byte

LRU Policy is used.

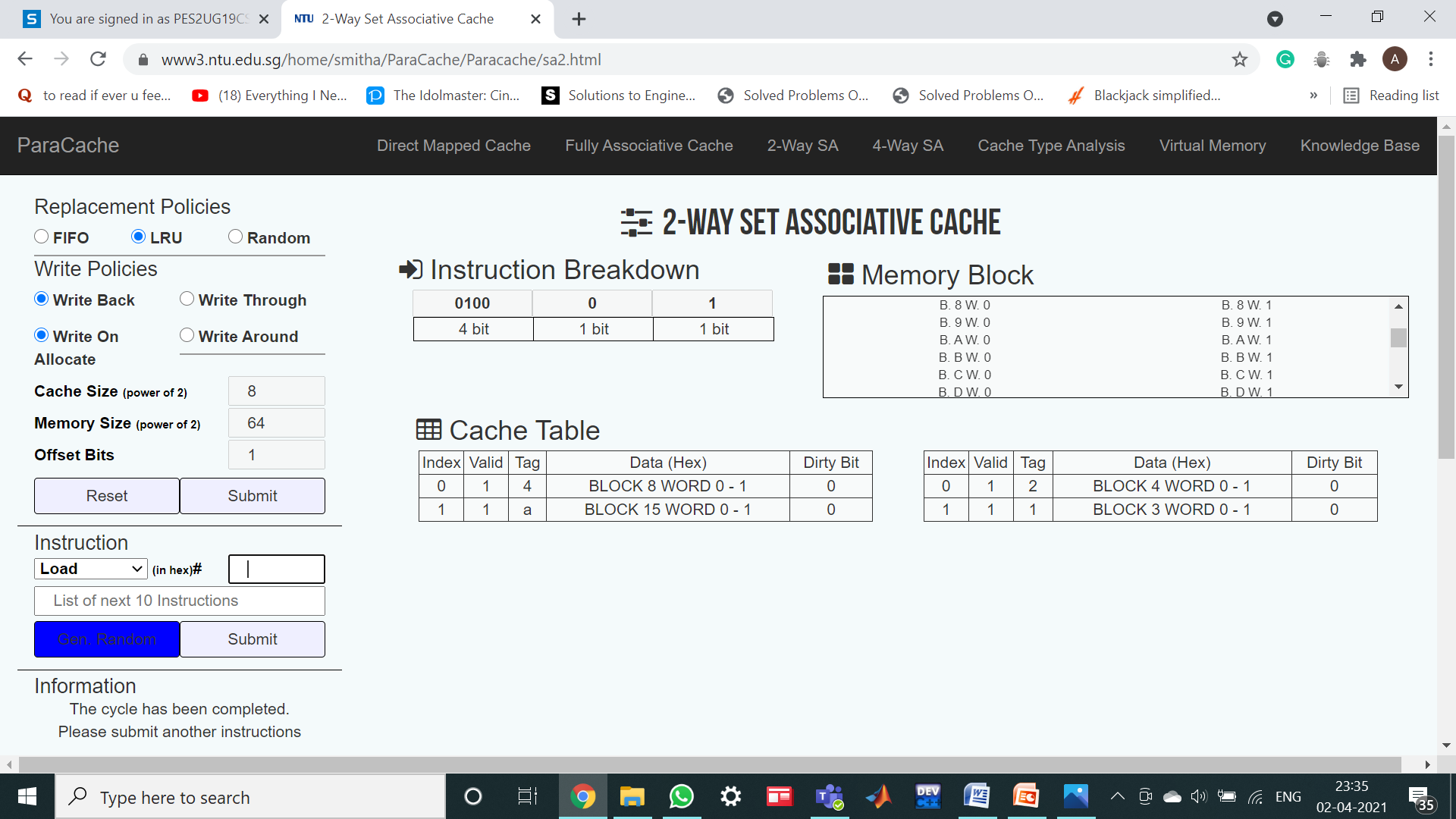
The cache is mapped as

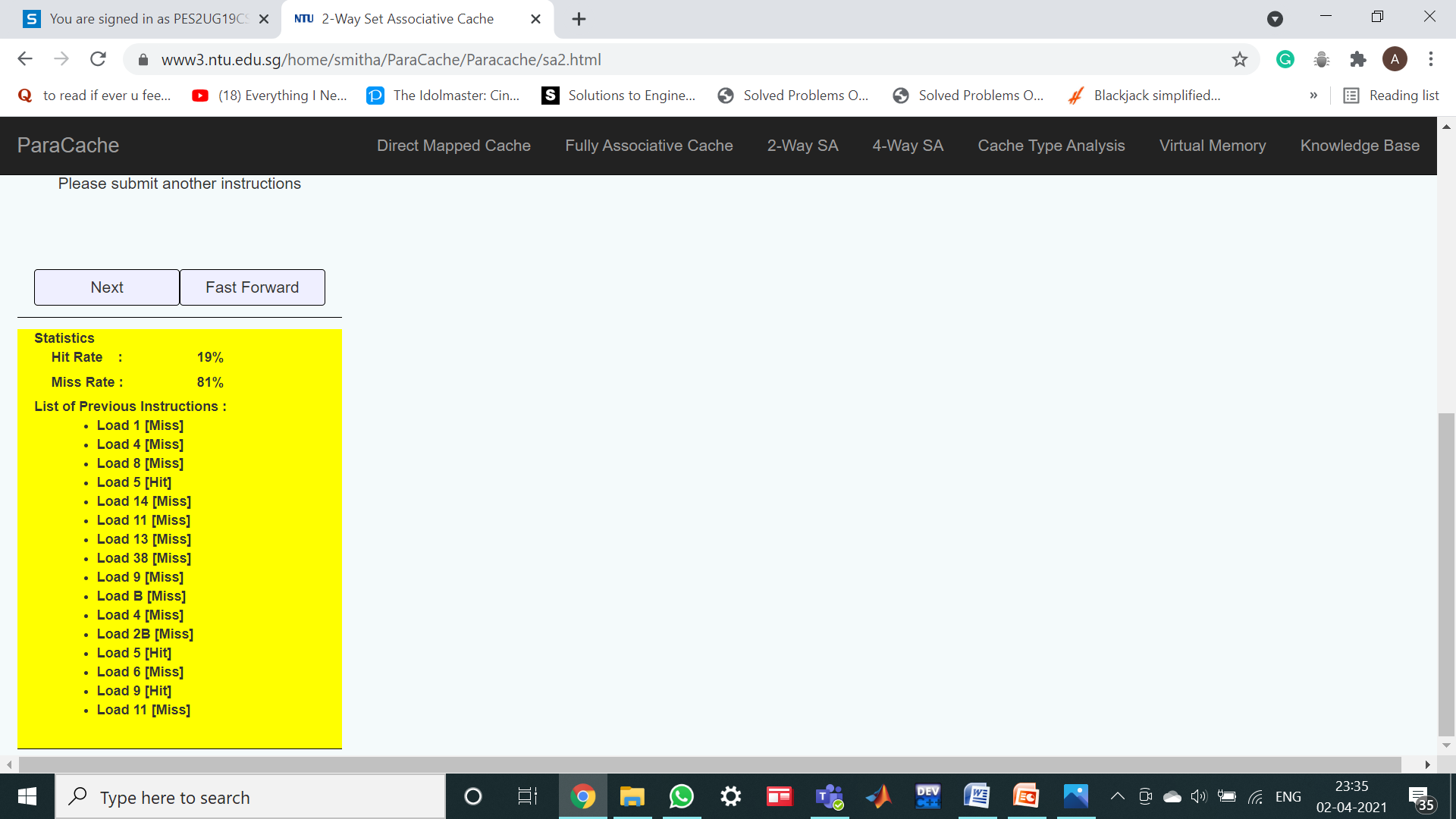
a)Direct Mapped



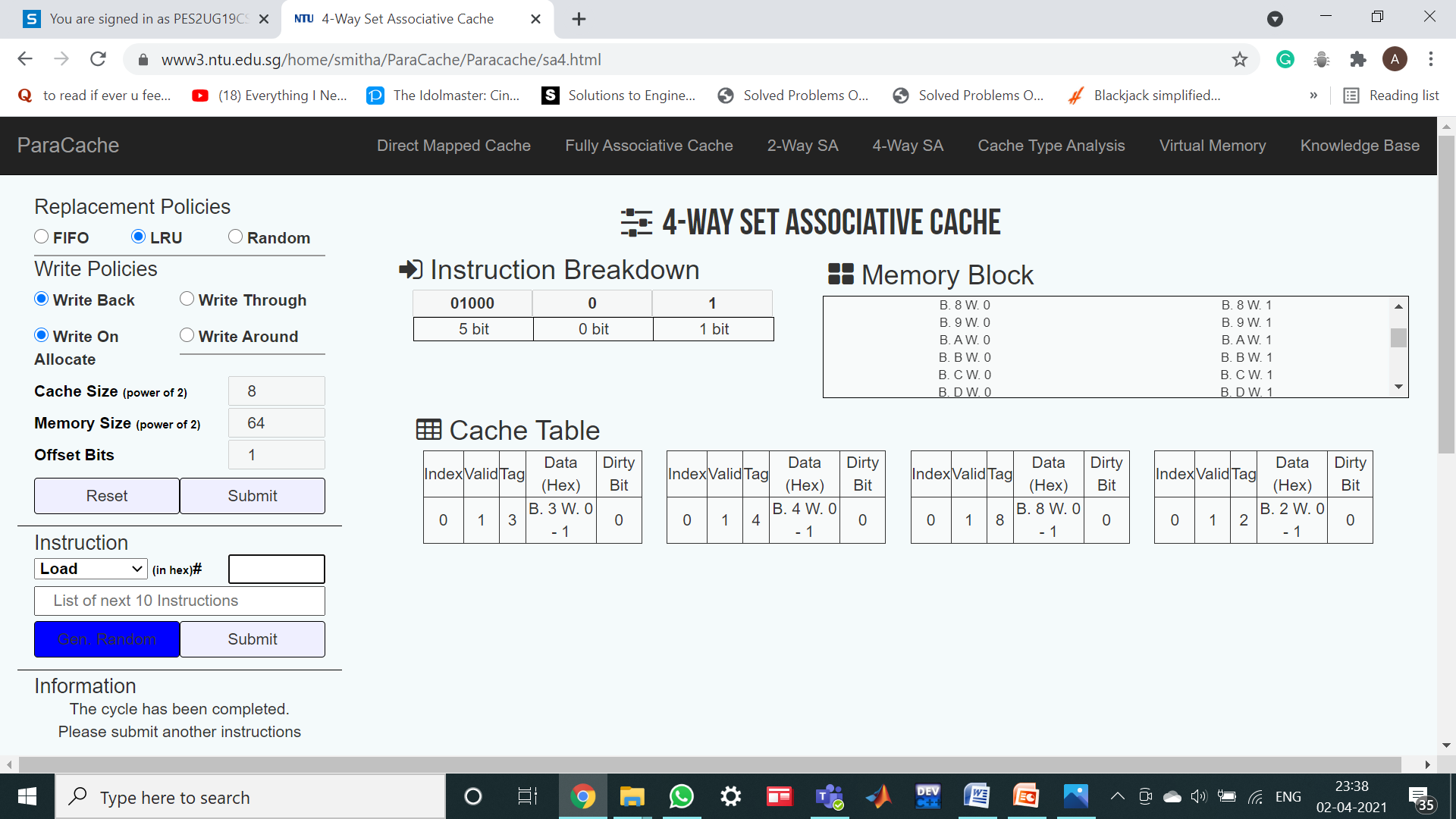


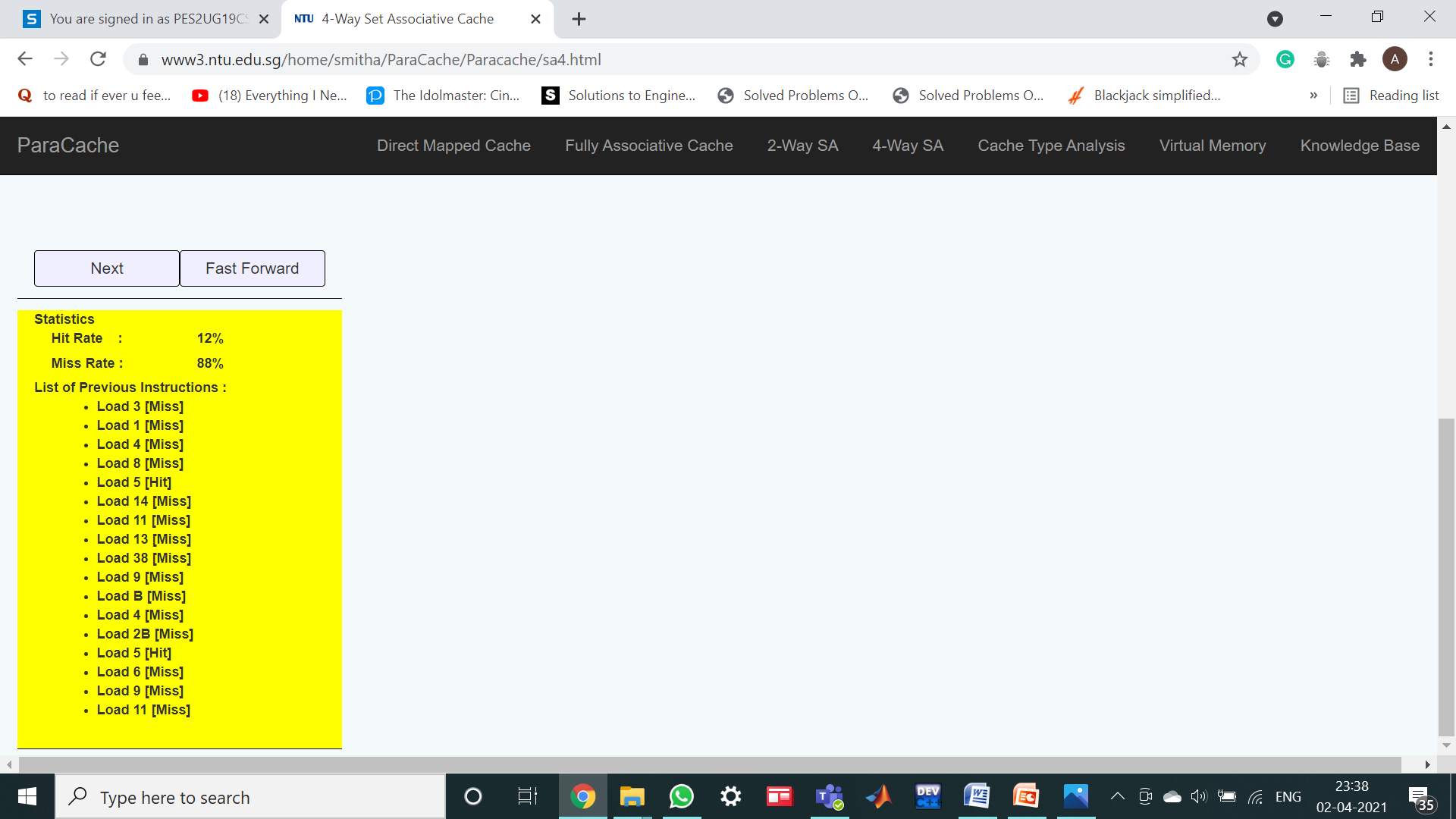
b)Two way set Associative



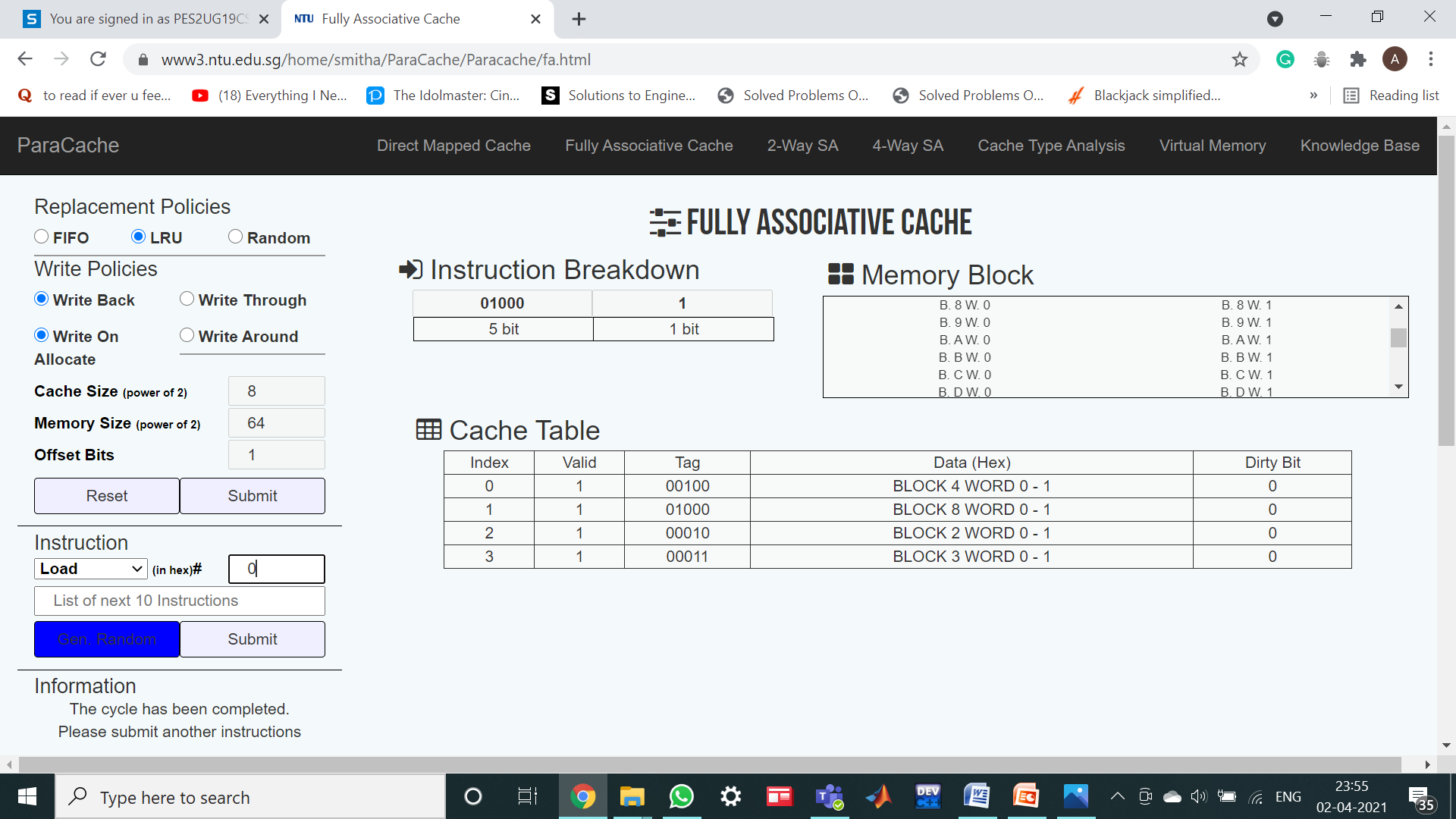


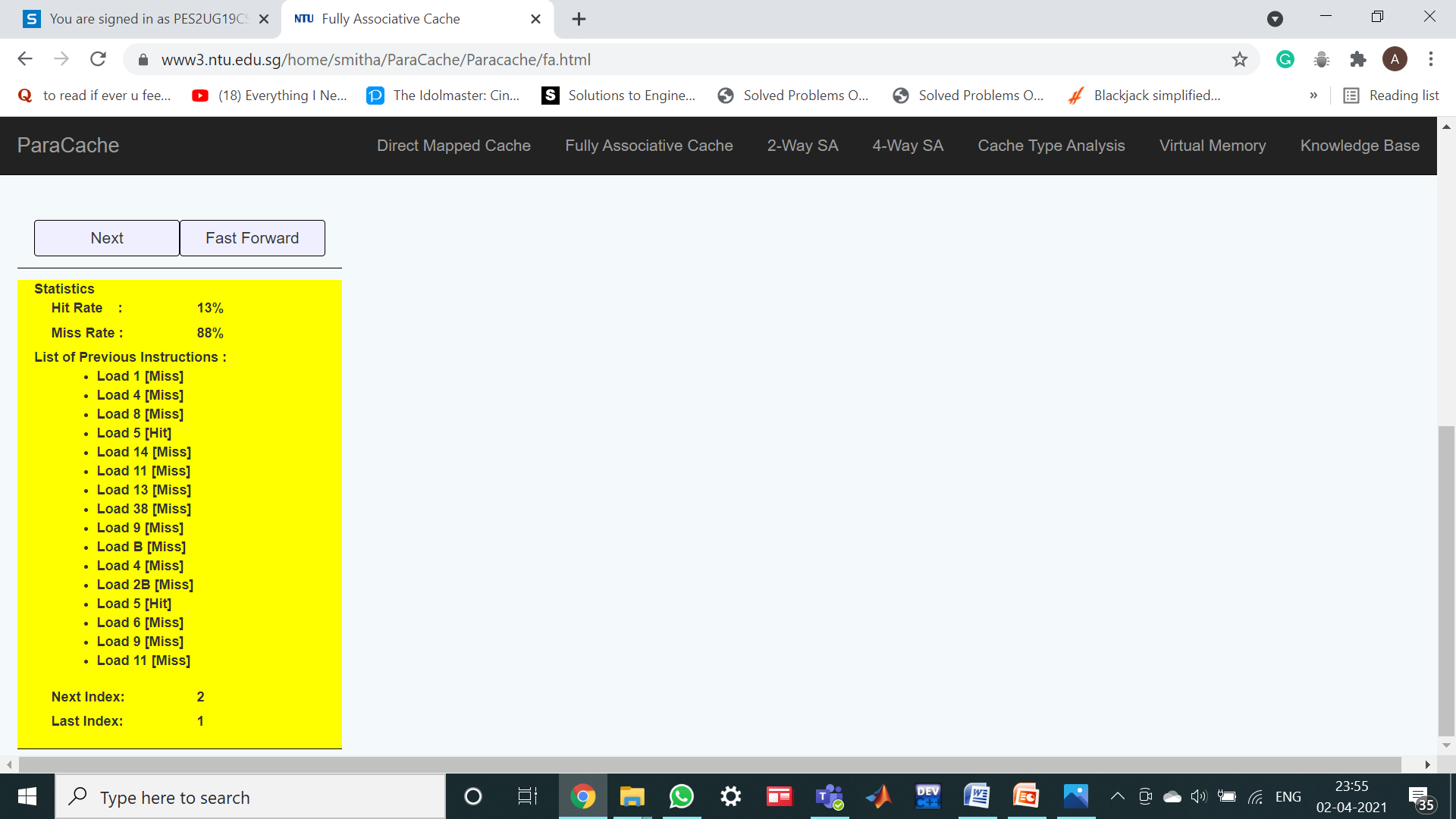
c)Four Way Set associative





d)Fully Associative

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